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IMPROVED MULTI-PHASE COUPLED INDUCTOR TOPOLOGIES

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ABSTRACT

Multi-phase pulse width modulation (PWM) of coupled inductor topologies provides a means of significantly reducing input and output filter capacitor size for a given ripple voltage requirement. Primary side filtering provides further reductions in capacitor size. Low profile magnetics and simple paralleled coupled inductor topologies yield designs with small size, low cost, high density, and high performance.

INTRODUCTION

The single ended flyback converter has the lowest parts count and is often the lowest cost candidate for a DC-to-DC converter design. The difficulties associated with this topology include: (1) the requirement for a large and costly output filter capacitor which must hold up the output during the on time of the primary switch and, therefore, must be capable of withstanding high ripple currents and (2) typically lower efficiency resulting from pulsating input and output currents which result in high peak current to average current ratios for both input and output currents and higher conduction and switching losses, in comparison to other topologies. As smaller and more efficient magnetic elements are developed the advantage of multi-phase systems becomes more attractive. In addition to reducing ripple and increasing efficiency the multi-phase low profile systems provide good thermal characteristics by distributing the heat sources over a wide surface area.

As high density planar magnetic elements become smaller and smaller, and capacitor and EMI filtering requirements are minimized with topological evolutions, the cost of power conversion will ultimately be driven by the power semiconductors. Because of the merits of multiple phase operation there is a need for a four phase integrated circuit controller which can be expanded to form 8, 12, or 16 phase controllers with ease.

MULTI-PHASE CONCEPT REVIEW

The advantages of a low profile multi-phase interleaved approach include: (1) reduced capacitance for a given ripple voltage, (2) higher efficiency resulting from lower conduction losses due to the inherent parallelism of the approach, (3) improved thermal characterisitcs accomplished by distributing the power losses over a wider area, (4) higher ripple frequencies for smaller, lighter, more efficient EMI filters, and (5) reduced volume of magnetic circuit elements since the power density capability of a magnetic circuit element increases for a given maximum hot spot temperature as the volume is reduced. For purposes of illustrating this last point Table 1 shows the power densities achievable at 500 kHz switching frequencies for standard size ferrite pot cores. These results are based upon the manufacturer's data. The results indicate a significant increase in power density as core size decreases.

Table 1

PACKAGE	AP (cm^4)	VOLUME(cm^3)	P (500 kHz)	P/V (500k)
1107	0.00815	0.251	11.6	46.3
1408	0.0244	0.49	23.2	47.4
1181	0.073	1.11	46.5	41.9
2213	0.0187	2.00	84.3	42.2
2616	0.392	3.5	134.7	38.4
3019	0.737	6.12	201	32.9
3622	1.53	10.7	319	29.8
4229	3.69	18.2	557	30.6

Two, four, and eight multi-phase systems are illustrated in Figures 1, 2, and 3. The principle of multi-phase control is to parallel the input and output connections of two, four, or eight separate DC-to-DC converters with a corresponding phase separation of 180°, 90°, or 45°, respectively. For a given total power level the pulsating currents in each separate converter is 1/2, 1/4, or 1/8 of the equivalent current of a single converter. The fundamental frequency of the ripple is two, four, or eight times the fundamental frequency of each single converter. Adding additional phases with a given input capacitance, output capacitance, and power will reduce the peak to peak fundamental ripple voltage inversely with the square of the number of stages. See Figure 4. For example, a two phase 100 watt converter operating at a frequency of 100 kHz requires two 50 watt converters with pulse width modulations staggered by 180°. If the ripple voltage of the converter is 100 mv peak to peak with a 10 micro-farad output capacitor, a four phase 100 watt converter could consist of four 25 watt 100 kHz converters with 90° phase shift with respect to each other. The ripple with the same 10 micro-farad capacitor is 25 mv and the input and output

ripple frequencies are 400 kHz. An eight phase system design will provide 6 mv of ripple with 800 kHz ripple frequencies.

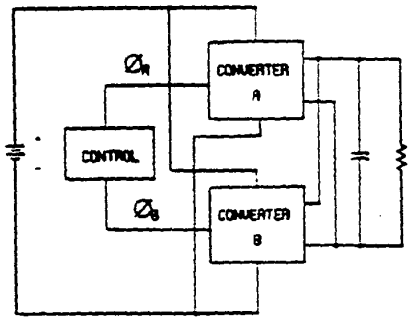

Figure 1. Two Phase Multi-Phase System

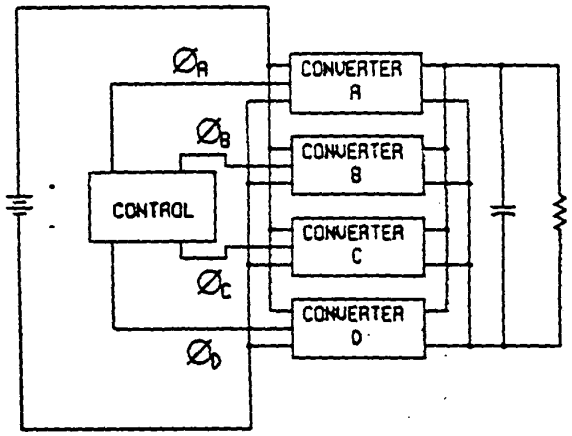

Figure 2. Four Phase Multi-Phase System

Another important consideration in the design of multi-phase systems is to provide sufficient phases for timing overlap between input and output conduction times. Especially with topologies which refer a filter capacitor through the coupled inductor to a low voltage output. A good rule of thumb is to determine the minimum conduction time of both the input and output semiconductors by considering the cases for maximum and minimum line voltage and minimum load, calculate the ratio of cycle time to minimum conduction time for each semiconductor and select a number of phases greater than that ratio. For example, if the worst case ratio of the cycle time to the rectifier conduction time is three, then select a minimum of four phases. If the worst case ratio at high line for conduction of the primary power switch is four, either a four or eight phase system will be adequate because timing overlap is mandatory for the output but may not be required for the input, depending on the ripple, noise, and EMI requirements for input and output.

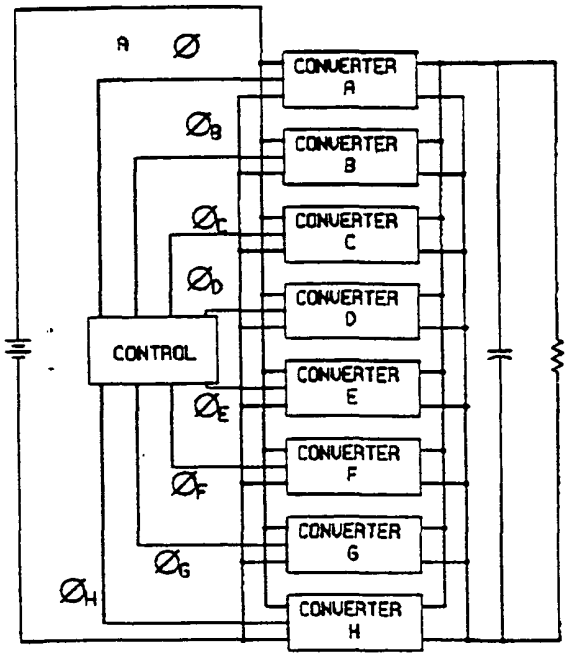

Figure 3. Eight Phase Multi-Phase System

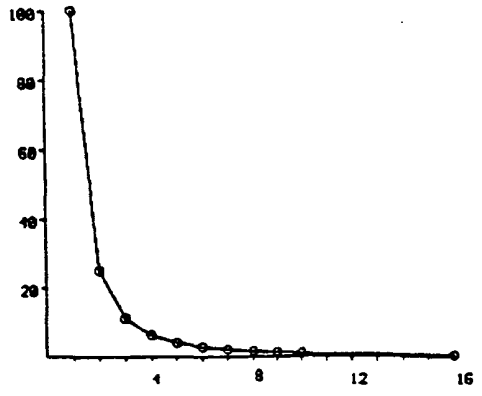

Figure 4. Ripple vs Number of Phases

TOPOLOGY REVIEW

In many cases a four or eight phase high density power system will be desirable - especially in the 100 to 200 watt power range. In order to provide the lowest overall parts count and consequently the highest reliability, the flyback topology is often a good choice for multi-phase systems. Figure 5 illustrates the flyback converter.

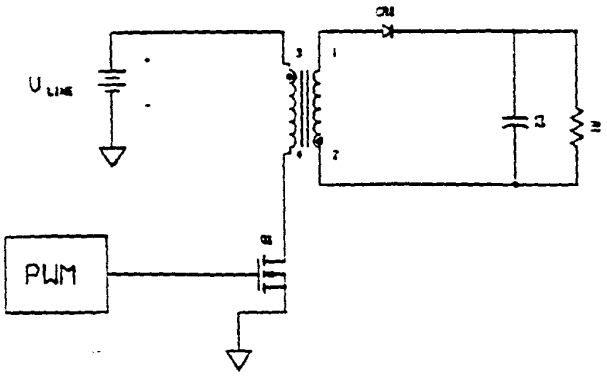

Figure 5. Flyback Converter

In a multi-phase system all input and output terminals are connected in parallel and the controller outputs are connected to the switches with a phase difference determined by the number of stages. For example, in a four phase system, the power switch gate drive will be staggered by 90°.

The input and output filtering requirement can be minimized by designing the transformer for continuous conduction (incomplete energy transfer). The impact of so doing requires that the current be sensed and current mode control be implemented. With a single loop voltage regulator and a discontinuous current design (complete energy transfer) of the transformer, line voltage feedforward can be implemented in the multi-phase controller without sensing the current. This is a simple and cost effective approach for obtaining good audio rejection.

One major cost driver in flyback converters is the output capacitor. Interleaving helps this situation considerably. The requirement for the output capacitor (neglecting ESR) for 10% ripple for a single phase system operating at 400 kHz and an output voltage of 5.0 v is 20 micro-farad per amp. A two phase system operating at 400 kHz is 5.0 micro-farad per amp. A four phase system reduces the total filter requirement to 1.25 micro-farad per amp. This is a significant number because a five volt output at 1.0 amp of current is 5.0 watts. There is a significant cost differential in a 1.0 micro-farad vs a 20.0 micro-farad ceramic capacitor. If the ceramic capacitor can be purchased for say $1.00/micro-farad, even with a four phase system the cost of the output filter capacitor is $.25 per watt. An eight phase system would reduce the capacitor by another factor of four to $.0625 per watt.

There is a pitfall however in assuming that multi-phase operation reduces filtering requirements to zero. With a small capacitor on the output of a multi-phase converter, the dynamic response to a transient load is lacking. One high density topology which can multiply the capacitor volume of a filter capacitor on the transformer primary by the turns ratio squared of the flyback transformer is illustrated in Figure 6.

The standard flyback converter with a switch (SW_2) connected to a capacitor (C_F) forms a new topology which improves the high frequency efficiency of the converter and provides support to the output terminals through the transformer

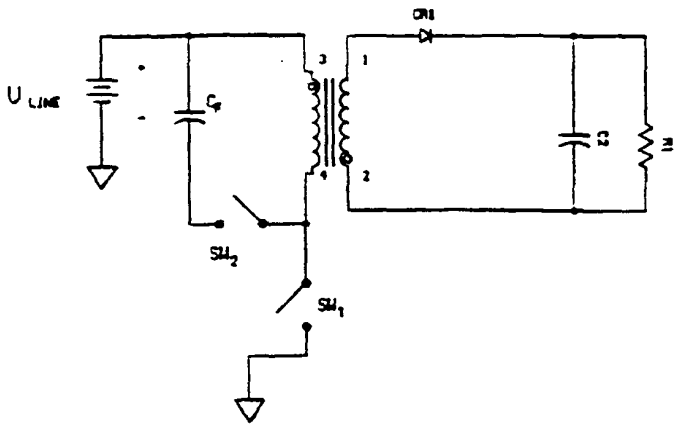

Figure 6. Primary Filtered Flyback

magnetic coupling for transient loads. Of course the path is broken when SW_2 opens and the rectifier diode is reverse biased. However in a multiple phase system the number of phases is chosen to insure that a least two of the multiple stages will overlap in time. This topology favors the use of ceramic capacitors because a turns ratio of six provides a multiplier of 36 for a 1 *micro*-farad 50 v capacitor.

Another feature of the topology is that the ESR of the capacitor as well as the $R_{DS\ ON}$ of the switch is reduced by the reciprocal of the turns ratio squared.

An alternative to the switched capacitor flyback topology is illustrated in Figure 7.

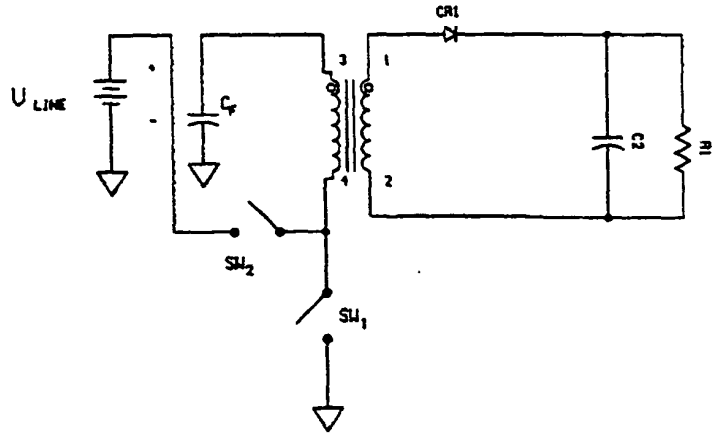

Figure 7. Switched Capacitor Coupled Forward Converter

In this circuit C_F is shared with the other identical converters operating at different phases in the switching cycle. With a 50% duty cycle on SW_1 and SW_2, the voltage on C_F is one half the line voltage, V_{IN}. The output voltage, neglecting the diode's forward voltage drop, will be one half the line voltage times the turns ratio of the coupled inductor. By paralleling outputs and using primary side filtering, as shown in Figure 5, the output filter capacitor can be significantly reduced or, perhaps,

eliminated. If, for example, the line voltage is 28 watts, the output voltage is 5 volts, and the coupled inductor has a three to one turns ratio then the impedanc of C_F at the output is 9 times (3 squared) less than its impedance on the primary side and for hold up and transients the capacitor requirement is one ninth of that required for secondary side filtering. Both the flyback and forward primary side filtering topologies require increased complexity of the controller for proper load sharing capabilities in multi-phase designs.

PRACTICAL CONSIDERATIONS FOR PLANAR MAGNETIC COUPLED INDUCTORS FOR 28 V AND 50 V INPUT APPLICATIONS

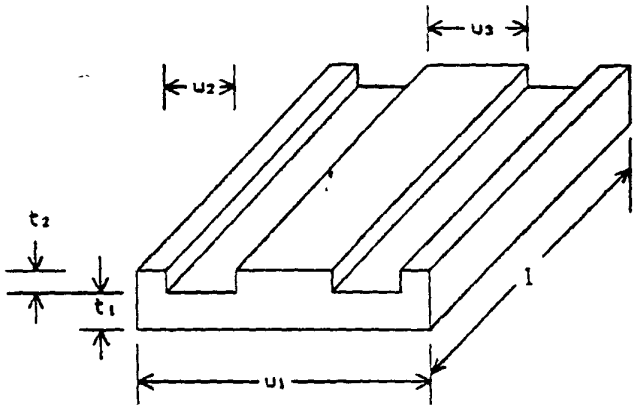

Figure 8. Planar E Core

In the design of a high density planar magnetic element, the following choices must be made.

1. What is a practical thickness of the return paths?
2. What is a practical thickness of the PC board?
3. What is a practical line width for the copper trace?
4. What is a workable transformer turns ratio?
5. What is the power capability of a practical design?
6. What is a practical length to provide good saturation flux density margins at a given operating frequency?
7. Would going to 1/2 of the operating frequency result in a violation of any of the choices?
8. What is the minimum number of layers?
9. What is the minimum spacing of windings?
10. What is the copper thickness?
11. Would going to a higher frequency result in a power density breakthrough for the design?

Recognizing that low profile is perhaps the most important physical parameter in a planar magnetic design, the thickness of the cover and return path is chosen based on the maximum height constraint of the design. If TO-220 transistors are used, 0.18 inches height is compatible with a magnetic element of the same

dimension and transistors mounted on the edge of a card. If a thickness of 0.050" is chosen, the maximum PC board thickness allowed including insulation is 0.080", with 0.005" spacing between 0.0028" copper, an eight layer board with 2 ounce copper and 0.005" spacing is approximately 0.057" thick. This allows 0.02" for insulation.

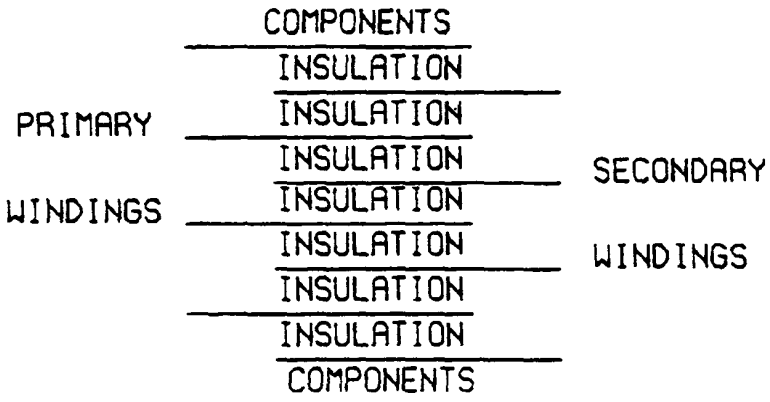

Figure 9. Primary Windings/Secondary Windings

If all of the layers are used in forming the windings and the primary windings are connected in series and the secondary windings are connected in parallel then, a turns ratio of four to one can be achieved. This is a workable turns ratio for a flyback converter because the 50% duty ratio occurs at 20 volts input.

The length of the planar "E" core is chosen based on the maximum allowable flux at the worst case duty ratio of the rectifiers - which is 1 - D_{MIN} of the power transistor, which at high line = 1 - 0.37 = 0.63.

For a 500 kHz converter the maximum time is 0.63 * 2 micro-sec = 1.26 micro-sec.

From Faraday's Law:

$$B = \frac{V \times 10^8 \, \Delta t}{2 \times A_E \, N}$$

$$\text{where } V = \text{output voltage} = 5.0\,V$$

$$\Delta t = 1.26\mu \text{ sec}$$

$$A_E = 0.1 \times 2.54 \times 1 \times 2.54$$

$$N = 1$$

$$B = 1000$$

$$\text{or } l = \frac{5.0 \times 10^8 \times 1.26 \times \Delta t \times 10^{-6}}{2 \times 1000 \times 2.54 \times 2.54 \times 0.1 \times 1} = 0.488 \text{ inches}$$

rounding l off to 0.5 inches. The width of the center post by definition is twice the cover thickness or 0.1 inches.

The line width of the trace in the transformer is chosen to be 0.05 inches. With 0.012" clearance on each side of the trace the PC board width between the center post and return path is 0.075 inches. The total width of the E core is the width of center post plus two times the width of the PC board or 0.1" + 0.1" +

0.15" = 0.35 inches.

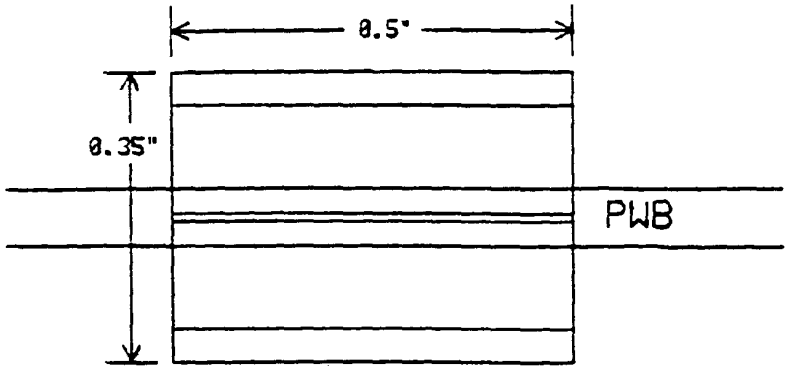

Figure 10. Planar Magnetic Element Optimized for 500 kHz Operation

The DC resistance of each winding can be calculated by multiplying the sheet metal resistance of two ounce copper, .25 x 10^{-3} ohm per square, by the number of squares (27 in this case). The resistance is 27 x 0.25 x 10^{-3} ohms = 6.75 x 10^{-3} ohms. The DC resistance of four output windings in parallel is 1.68 x 10^{-3} ohms.

Calculating the core loss - The core loss of C8MX material is 0.7 watts/cm^3 @ 1000 gauss and 500 kHz. The volume of the ferrite is (0.5 x 0.35 x 0.18) - (2 x 0.075" x 0.08" x 0.5") = 0.03 - 0.006 = 0.024 in^3 or 0.39 cm^3. The core loss at high line is 0.27 watts.

The optimum efficiency of the transformer is for equal copper and core losses - calculating the maximum current corresponding to 0.27 watts of core loss,

$$I = \sqrt{\frac{0.27}{1.68}\ 10^3} = 12.6\ amps$$

The average output current is 12.6 amps times the duty ratio of 0.63 or 7.98 amps - (approximately 8 amps). This corresponds to an output of 40.0 watts.

The efficiency of the transformer is

$$\frac{40.0}{40.0 + (2 \times 0.27)} = 98.66\%$$

The power density of the magnetic element is defined as the ratio of the power processed by the element to the volume of the element in cubic inches or 40/0.037 = 1058 watts/in^3. This is an important number because the volume of a DC to DC converter can never be better than this number at this operating frequency.

The preceding analysis is interesting because in a multi-phase system with four phases, the volume of the input and output filter capacitors virtually disappear and a 40 watt magnetic element is about the size of a 14 pin plastic IC DIP with an internal power dissipation of less than one watt.

CONCLUSION

Multi-phase single coupled inductor topologies designed with high coupling coeffient reduce magnetic and capacitor volume significantly compared with single phase systems. Thermal characteristics of multi-phase systems are superior to single-phase systems because of the distributed nature of the semiconductors and magnetic elements. In addition, multi-phase single coupled inductor topologies with a primary capacitor referred to the output through a switch commutated synchronously with the output rectifier provides superior transient response for a given volume of filter capacitance. The challenge for achieving high efficiency at high power levels, high frequencies, and low output voltage is to minimize the lead inductance of the rectifier elements. The effect of lead inductance is to increase turn on and turn off transition times. For non-resonant transitions this leads to increased switching losses. For both non-resonant and resonant transitions lead inductances contribute significantly to reduced effective duty cycle at high frequencies. Furthermore expandable multi-phase controllers with four staggered outputs controlled from a stable high frequency source are required to reduce the number of IC chips required with currently available CMOS derived controllers.

In summary, this paper has addressed some significant issues relating to high power density. Those issues include power density of magnetic circuit elements, capacitor volume, and number and size of power semiconductor devices. The solutions suggested here would increase the power density of the magnetic circuit elements by effectively paralleling the magnetic elements in a multi-phase interleaved design, using more elements where each element handles a fraction of the power but also achieves higher power density. Capacitor volume and cost is significantly decreased by interleaving which reduces ripple currents and multiplies the ripple frequency and by using primary side filtering which further reduces the capacitor requirement by the square of the turns ratio. The number of required power semiconductors increases but the power handling requirements of each power semiconductor is reduced so that smaller packages could be used which reduces the impact of the parts count problem. The thermal problems are also reduced by distributing the losses over a large area. The topological solutions proposed here use a minimum number of circuit elements in the primary power path of the individual converters. This factor is critical to any design which seeks to achieve high power density and cost effectiveness. One problem remaining with the solutions proposed here in the multi-phase interleaved approach is the complexity and parts count of the system controller. This problem is significant but the technology to solve this problem is at hand in integrated circuit semiconductor device technology. Application specific ICs could be fabricated today to reduce the significance of this problem and monolithic devices could be developed in the near future.